

## **Personal details**

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## **Summary**

Mixed-signal IC designer/hardware engineer currently working on high-speed chip-to-chip interface circuit design at MediaTek. Previously served at a start-up company – BioPro Scientific on neuroscience instrumentation and electrical therapy for neurological disorders. Prior to BioPro, a PhD researcher at EPFL, Switzerland. The PhD project consists of ASIC/PCB design as well as MEMS/IC integration in collaboration with a start-up medical device company (Aleva Neurotherapeutics SA) for a new deep-brain-stimulation product. Wide coverage of hardware development from a complex mixed-signal ASIC to PCB design and FPGA coding. 3-year industrial experience as a design engineer at TSMC and AMD before PhD. Successful silicon development experiences in various technology including 0.35 $\mu$ m, 0.18 $\mu$ m, 28nm, 20nm, 16nm, 10nm and 0.18 $\mu$ m BCD. Strong analytical skill and high-level system modeling capability using simulation tools with different abstractions.

## **Technical interest**

- Low-power, low-noise circuits and systems for biomedical and generic sensor interfaces.
- I/O circuits and ESD protection.
- Automotive electronics.
- High-speed analog/digital design

## **Education**

- 2014.12~2018.08: Doctor of Philosophy, *Microsystems and Microelectronics, Swiss Federal Institute of Technology in Lausanne, Switzerland*. PhD thesis: "System Design and Advanced Circuit Techniques for Bi-Directional Brain-Machine Interfaces".
- 2009.09~2011.07: Master of Science, *Institute of Electronic Engineering, National Tsing Hua University, Taiwan*. Master thesis: "A CMOS FET sensor chip to detect the DNA amplification process".
- 2005.09~2009.06: Bachelor of Science, *Department of Electrical Engineering, National Tsing Hua University, Taiwan*.

## **Experience**

- 2019.10 ~ present: Technical manager, MediaTek, Hsinchu, Taiwan
- 2018.10 ~ 2019.10: Deputy manager, BioPro Scientific Co. Ltd., Hsinchu, Taiwan
- 2014.12~2018.08: Research assistant, Microsystems and Microelectronics program, Swiss Federal Institute of Technology in Lausanne (EPFL), Lausanne, Switzerland
- 2014.05~2014.11: Contractor, Electronic Design Division, Advanced Micro Devices, Sunnyvale, California, USA
- 2011.10~2014.11: Design Engineer, Design & Technology Platform, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

## **Skill**

- Programming Languages
  - C/C++, Matlab, Perl, Python, Verilog, Verilog-A, Ocean
  
- Full-custom IC design EDA tool
  - HSPICE, Cadence, Spectre, Laker, Virtuoso, Calibre, StarRC, Totem
  
- Semi-custom IC design EDA tool
  - Sigasi, Modelsim, Design Vision
  
- PCB
  - Altium, KiCAD

## **Major Achievement at Mediatek**

- Low-power DDR PHY TX/RX design using 5nm FinFET technology
- Architecture exploration of decision-feedback equalizers for DDR PHY and ultra-short reach chip-to-chip interconnect
- STA flow build-up for high-speed digital signoff

## **Major Achievement at Biopro**

- Design and test of a low-noise analog-frontend for neural recording.
- Design and test of a current-mode neural stimulator including:
  - Negative supply voltage generation using a pulse-frequency modulated charge pump.
  - 10-bit current DAC.
  - Overdrive current driver free of reliability issues
- Data analysis of recorded signals from rats (FFT, time-frequency analysis....).
- Characterization of different analog blocks (SAR ADC, Wireless power, LDO....).

- PCB design/debug. Component evaluation and selection.
- Patent writing.

### **PhD Project Description**

- Design a miniaturized hardware for an MRI compatible deep brain stimulation system in collaboration with Aleva Neurotherapeutics – a startup company focused on MEMS technology for deep brain stimulation. The project consists of the following parts:
  - An ASIC which includes low-noise instrumentation amplifiers, ADCs, a high-voltage compliant stimulator, a digital controller and power management units for a bi-directional, multi-channel neural interface.
  - Electrical-optical interface to tackle the noise issue induced by MRI equipment
  - FPGA/PC interface implementation. Signal analysis.
- Explore energy-efficient stimulator design based on a high-frequency switched capacitor scheme.
- Time-based analog front-end for neural recording and generic sensor interfaces.

### **Major Achievement at TSMC**

- Design and validation of a transceiver circuit with full ESD protection using a 0.18 $\mu$ m BCD process to meet FlexRay automotive standard.
- Design and validation of a low power crystal oscillator with automatic gain control for mobile applications using 28nm and 16nm technologies.
- Develop a full-custom, simulation-based ESD design flow based on Verilog-A behavior model.
- Deliver the roadmap GPIO library in 20nm technology.
- Deliver the first GPIO library in 10nm technology for SRAM yield learning.

### **Major Achievement at AMD**

- GDDR5 circuit design for several blocks (CTLE, impedance calibration, clock trees, serializer....) using 16nm FinFET technology.
- CAD support for AMD internal EM/IR flow.

## Publication

- Wen-Yang Hsu, Ping-Hsuan Hsieh and Hsin Chen, " Design Considerations for Implantable Neural Circuits and Systems," to appear, Chapter in Springer Handbook of Neuroengineering, edited by Nitish V. Thakor, 2020.
- Wen-Yang Hsu, Daniel Mathias Bold and Alexandre Schmid, "Design and Analysis of a Low-Voltage, Low-Power, Time-Based Analog Front-End Aiming at Wireless Neural Recording", major revision, *Analog Integrated Circuits and Signal Processing*
- Hsu, W.Y. and Alexandre Schmid, "Compact, Energy-Efficient High-Frequency Switched-Capacitor Neural Stimulator with Active Charge Balancing", in IEEE Transactions on Biomedical Circuits and Systems, Aug. 2017, Volume 11, Issue 4, pp 878-888
- Hsu, W.Y., Cao C, and Alexandre Schmid, "A Time-Based, Digitally Intensive Circuit and System Architecture for Wireless Neural Recording with High Dynamic Range", IEEE International Midwest Symposium on Circuits and Systems, Abu Dhabi, UAE, 2016
- Hsu, W.Y., Lan, P.H., Lin, W.Y., Lee, J.W., Chen, K.J., and Song, M.H. "A Highly Reliable, Self-Isolation Current-Mode Transmitter (CM-TX) for +60V Automotive Interface with Bulk BCD Technology", Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), Tucson, Arizona, USA, 2014
- Lin M.Y., Hsu, W. Y., Yang, Y.S., and Chen, H. " Immobilized rolling circle amplification on extended-gate field-effect transistors with integrated readout circuits for early detection of platelet-derived growth factor ", Analytical and Bioanalytical Chemistry, July 2016, Vol 408, Issue 17, pp 4785–4797
- Lee, Y.C., Hsu, W.Y., and Chen, H. "A Compact Gm-C Filter Architecture with an Ultra-low Corner Frequency and High Ground-noise Rejection", IEEE Biomedical Circuits and Systems Conference, Rotterdam, Netherland, 2013
- Wang, Z.Y., Hsu, W.Y., Chen, Y. C., and Chen, H., "A Low-noise, Low-offset, Micropower Instrumentation Amplifier for Chronic Recording of Neural Field Potentials", the Symposium on Engineering, Medicine, and Biology Applications (SEMBA), 2013
- Chen, Y. C., Lin, Y. P., Hsieh, T. L., Yeh, C. Y., Huang, P. Y., Chiu, H.C., Zong-Ye Wang, Z. Y., Hsu, W. Y., Huang, P. C., Tang, K. T., Ma, H. P., Chen, H. "An Implantable Microsystem for Studying the Parkinson's Disease", IEEE Asia Pacific Conf. on Circuits and Systems, Kaohsiung, Taiwan, 2012

## Patent

- Hsu, W.Y., and Lee, C.Y. "High Voltage Protection Apparatus and Method", US8829947
- Chen, G.Y. and Hsu, W.Y., "Oscillator Circuit and Related Method", US9306495

## Reviewer

- **Journal:** IEEE Transactions on Circuits and Systems II: Express Briefs
- **Conference:** IEEE biomedical circuits and systems conference

## **Awards and Honors**

■ Q3.2013: Outstanding Procedure Innovation Award, awarded by Design and Technology Platform, TSMC

Title: Full-custom ESD design flow based on Verilog-A behavior model

■ 2013.08: Runner-up paper award, awarded by TSMC DTP conference

Title: High-Voltage Tolerant, FlexRay-Compliant Transmitter Design with Bi-directional ESD Clamp

■ Outstanding Student Scholarship NT\$60000, awarded by the College of Electrical Engineering and Computer Science, *National Tsing Hua University*